AMENDMENTS TO THE CLAIMS

Claims 32-38 are pending in the present application. Claims 32, 33, 35 and 37-38 have amended as set forth below. Claims 34 and 36 have been canceled. Claims 47-55 have been added. This listing and version of the claims replace all prior listing and versions of the claims.

Listing of Claims:

1-31. (Canceled)

32. (Currently amended) An integrated vertical multiple npn transistor ESD protection structure on a semiconductor substrate, functionally connected between an integrated circuit input or output pin and ground ~~which will prevent~~for preventing electrostatic discharge damage to said integrated circuit comprising:[[;]]

a first semiconductor layer having a first conductivity ~~dopent~~dopant type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different ~~dopent~~dopant concentration;

a third semiconductor layer having a second conductivity ~~dopent~~dopant type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity ~~dopent~~dopant type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a top element making electrical contact to said second regions and said second semiconductor layer; and

a plurality of third regions of said first semiconductor layer conductivity ~~dopent~~dopant type laterally spaced and interposed between said second regions,[[;]]

wherein said third regions are arranged in an alternating array within said third semiconductor layer, with "N" number of said third regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure, and

wherein one of said second regions of said second conductivity dopant type is disposed between said alternating array and a top one of said first regions and, and another of said second regions is disposed between said alternating array and a bottom one of said first regions.

33. (Currently amended) The ESD protection structure of claim 32 whereby the plurality of said first regions together with the associated connected first semiconductor layer are with n ~~dopent~~dopant and form multiple collector elements of a bipolar transistor in which the bases are formed by said third conductivity layer and associated said plurality of said second regions of p ~~dopent~~dopant, and by which multiple emitter elements are formed by said plurality of ~~laterally spaced~~ third regions of n type ~~dopent~~dopant.

34. (Canceled)

35. (Currently amended) The ESD protection structure of claim 32 whereby said first ~~collector~~ regions have horizontal contact conductor stripes at the top and bottom of said transistor array which are ultimately connected together and to a first voltage source of said integrated circuit input/output pin.

36. (Canceled)

37. (Currently amended) The ESD protection structure of claim 32 whereby said third ~~semiconductor emitter~~ regions are electrically connected by a conductor element with N

horizontal stripe conductor elements and connected in a contiguous box like manner by vertical contact conductor elements at both ends of said horizontal emitter conductor stripes.

38. (Currently amended) The ESD protection structure of claim 32 whereby said ~~plurality of~~ second ~~semiconductor base~~ regions ~~electrical contact conductor elements~~ and said third ~~semiconductor emitter~~ regions ~~electrical contact conductors~~ are ultimately connected together and to a second voltage source~~, typically ground~~.

39-46. (Canceled)

47. (New) The ESD protection structure of claim 38, wherein the second voltage source is ground.

48. (New) The ESD protection structure of claim 32, wherein the third regions are electrically connected by a conductor element with N horizontal stripe conductor elements, and at least two of the horizontal stripe conductor elements are connected by at least one first vertical contact conductor element at one end of the horizontal stripe conductor elements, and at least two of the horizontal stripe conductor elements are connected by at least one second vertical contact conductor element at another end of the horizontal stripe conductor elements so that the horizontal stripe conductor elements are electrically connected to each other.

49. (New) An integrated vertical multiple npn transistor ESD protection structure on a semiconductor substrate, comprising:

a first semiconductor layer having a first conductivity dopant type;

a second semiconductor layer overlying the first semiconductor layer, having a similar conductivity type as the first layer, but a different dopant concentration;

a third semiconductor layer having a second conductivity dopant type opposite that of the first semiconductor layer, disposed in overlying relation to the second semiconductor layer;

a plurality of first regions of the first conductivity type electrically connecting with the first semiconductor layer, having a top element making electrical contact to the first regions and the first semiconductor layer;

a plurality of second regions of the second conductivity dopant type laterally spaced from the first regions, being electrically connected to the third semiconductor layer having a top element making electrical contact to the second regions and the second semiconductor layer; and

a plurality of third regions of the first semiconductor layer conductivity dopant type laterally spaced and interposed between the second regions,

wherein the third regions are arranged in an alternating array within the third semiconductor layer, with "N" number of the third regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array, and

wherein one of the second regions of the second conductivity dopant type is disposed between the alternating array and a top one of the first regions, and another of the second regions is disposed between the alternating array and a bottom one of the first regions.

50. (New) The ESD protection structure of claim 49, wherein the plurality of the first regions together with the associated connected first semiconductor layer are with n dopant and form multiple collector elements of a bipolar transistor in which the bases are formed by the third conductivity layer and associated the plurality of the second regions of p dopant, and by which multiple emitter elements are formed by the plurality of the third regions of n type dopant.

51. (New) The ESD protection structure of claim 49, wherein the first regions have horizontal contact conductor stripes at the top and bottom of the transistor array which are ultimately connected together and to a first voltage source of the integrated circuit input/output pin.

52. (New) The ESD protection structure of claim 49, wherein the third regions are electrically connected by a conductor element with N horizontal stripe conductor elements and connected in a contiguous box like manner by vertical contact conductor elements at both ends of the horizontal emitter conductor stripes.

53. (New) The ESD protection structure of claim 49, wherein the plurality of the second regions and the third regions are ultimately connected together and to a second voltage source.

54. (New) The ESD protection structure of claim 53, wherein the second voltage source is ground.

55. (New) The ESD protection structure of claim 49, wherein the third regions are electrically connected by a conductor element with N horizontal stripe conductor elements, and at least two of the horizontal stripe conductor elements are connected by at least one first vertical contact conductor element at one end of the horizontal stripe conductor elements, and at least two of the horizontal stripe conductor elements are connected by at least one second vertical contact conductor element at another end of the horizontal stripe conductor elements so that the horizontal stripe conductor elements are electrically connected to each other.